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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,649	09/28/2001	Jeoff M. Krontz	1662-34100 JMH (P00-3058)	5226

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,649	KRONTZ ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-13,18,27,31 and 32* is/are rejected.

7)☒ Claim(s) *2-4,14-17,19-26 and 28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: Google™ search: define clock (one sheet)

DETAILED ACTION

Claim Objections

1. Claims 1, 12, 26 and 27 are objected to because of the following informalities:

As to Claim 1, line 12: "a" (occurring after "least") should be deleted.

As to Claim 1, line 13: –of– should be inserted after "length".

As to Claim 12, line 2: "select" should be changed to –selected--.

As to Claim 19, line 12: "of the" should be deleted because it repeats the phrase in line 11.

Claims 20-25 depend from Claim 19 and therefore inherit the defect of the claim.

As to Claim 26, line 11: –is– should be inserted after "pad".

As to Claim 27, line 20: "a" (occurring after "least") should be deleted.

As to Claim 27, line 20: –of– should be inserted after the second occurrence of "length".

Appropriate correction is required.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Hong (US 6,281,838 B1) Osaka et al. (US 6,034,878)

Delzer (US 6,734,757 B2) LaBerge (US 6,763,416 B1)

Google™ Search definition of "clock" on the Internet (one sheet attached to the present Office Action with the definition indicated by Examiner's annotation in red ink).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 6-13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong in view of Delzer and the above-cited definition of "clock" found on Google™.

A) As to Claim 1:

I. Hong discloses, in Fig. 3: a signal source (connected to input line 40; col.4: 3: 65-66); a signal destination (radiating element) connected to output line 12 (col.4: 54-57); a signal path 30 having a length, the signal path coupling the signal source and the signal destination, comprising: a first plurality of signal paths 34a,b,c each having two ends, a source end of a selected (i.e., any one) path of the first plurality of signal paths 34a,b,c, coupled to the signal source (through input line 40; Fig. 3 and col.4: 6-11); a second plurality of signal paths 58a,b,c (the designations a,b,c added by the Examiner and corresponding to each line of stage 32d, as in lines 34a,b,c in stage 32a) each having two ends, a destination end of a selected (i.e., any one) path of the second plurality of signal paths 58a,b,c, coupled to the signal destination (Fig. 3; col.4: 54-57 and col.5: 1-11); a spanning circuit (stages 32b and 32c) coupling the selected path of the first plurality of signal paths 34a,b,c to the selected path of the second plurality of signal paths 58a,b,c (Fig. 3 and col.4: 44-57); and wherein the length of the signal path

is at least the sum of a length of the selected path of the first plurality of signal paths 34a,b,c and a length of the selected path of the second plurality of signal paths 58a,b,c (Fig. 3).

II. Hong teaches a transmission signal from the signal source at input line 40 (col.3: 63-67) steered through the stages 32a-d of the signal path 30 to the transmission signal destination 12 in order to perform a phase shift delay of the signal. Hong does not teach that this transmission signal is a control signal in a computer system.

III. Delzer discloses a clock signal from a signal source connected to port P1, through delay paths determined by conductors 12 selectively connected by zero ohm connectors 20 in an adjustable delay line phase shifter. A clock signal is an old and well-known control signal, as evidenced by the following definition of a clock provided in the glossary web-site: "Any of several types of timing control devices, or the periodic signals that they generate." [See Google™ Search attachment] and www.tagnet.org/digitalhymnal/en/glossary_a-l.html.

IV. Since Hong and Delzer are both solving the same type of signal propagation problem, wherein a signal needs to be delayed using selected paths determined by zero-ohm connectors or switch contacts, then the use of such an adjustable delay line phase shift circuit for a control signal on a high frequency circuit board, as taught by Delzer, for use in any high frequency application, such as in a computer environment, would have been readily recognized in the pertinent high frequency electronics art of Hong.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the high frequency communication signal in Hong to be a control signal, specifically, the clock signal taught by Delzer, in order to use the various delay paths in Hong for selectively determining the precise phase delay for the control (clock) signal required by the particular electronic application of the delay circuit of Hong, as taught by Delzer.

B) As to Claim 6:

I. Hong, as modified by Delzer, teaches a control signal source that is phase shifted for outputting a signal with a calibrated delay for an application (see the rejection of base Claim 1, above) but does not establish the use of a phased lock loop (PLL) as claimed in Claim 6.

II. However, Delzer further discloses, in Fig. 7, that the control signal source is a feedback output (at amplifier 88) of a PLL, the control signal destination (at phase detector 74) is a feedback input of the PLL, the control signal path is a feedback path of the PLL (the PLL path defined by the path that includes phase shifters 10), and the length of the feedback path (defined by the specific path lengths formed on the adjustable phase shifters 84 and 90) controls a phase relationship between an input signal to the PLL and an output signal of the PLL in order to precisely control the delay of the control signal for an application (Fig. 7; col.4: 61-col.5: 40).

III. Since Hong, as modified by Delzer, are both teaching an adjustable delay line phase shifter for propagating a source control signal to a control signal destination for the purpose of precisely controlling the delay of a control signal for an application, then

the establishment of a PLL, the output of which is the control signal source and the input of which is the control signal destination, and the feedback path of which is the control signal path, the length of which path being adjustable and controlling the phase relationship of the input signal to and output signal from the PLL for use in an electronic application requiring such a precisely timed signal, as taught by Delzer, would have been readily recognized for use in conjunction with the adjustable delay line phase shifter in the pertinent art of Hong.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the adjustable delay line phase shifter circuitry of Hong with an added PLL, as taught by Delzer, in order to precisely control the phase relationship between an input signal to the PLL and an output signal of the PLL, as taught by Delzer, for the purpose of outputting a precisely timed signal for use in an electronic application of the adjustable delay line phase shifter circuitry of modified Hong, as taught by Delzer.

C) As to Claim 7, modified Hong further discloses at least two of the first plurality of signal paths 34 have different lengths (Hong: Fig. 3 and col.4: 6-11).

D) As to Claim 8, modified Hong further discloses at least two of the second plurality of signal paths 58 have different lengths (Hong: see paths 58 in Fig. 3 and discussion in col.4: 6-11).

E) As to Claim 9, modified Hong further discloses each of the first plurality of signal paths 34 have different lengths (Hong: Fig. 3 and col.4: 6-11).

F) As to Claim 10, modified Hong further discloses each of the second plurality 58 of signal paths have different lengths (Hong: see paths 58 in Fig. 3 and discussion in col.4: 6-11).

G) As to Claim 11, modified Hong further discloses each of the first and second plurality of signal paths have different lengths (Hong: see paths 34 and 58 in Fig. 3 and discussion in col.4: 6-11).

H) As to Claim 12, modified Hong further discloses that lengths of each of the signal paths 34 and 58 in the first and second plurality of signal paths are selected so that each unique path through the control signal path has a unique length (Fig. 3; col.4: 58-col.5: 13).

I) As to Claim 13:

I. Hong discloses coupling an adjustable signal path circuit 30 having a plurality of possible signal path lengths between the signal source (at input line 40) and the signal destination (at output 12); adjusting a length of a signal path through the adjustable signal path circuit to selectively add time delay to the signal comprising: selecting a first signal path in a first cluster of possible signal paths 34, the first signal path having a length; selecting a second signal path in a second cluster of possible signal paths 58, the second signal path having a length; coupling the first and second signal paths; and forcing the signal to propagate along the overall signal path having a length comprising the first and second signal paths (col.4: 58-col.5: 13).

II. Hong teaches a transmission signal from the signal source at input line 40 (col.3: 63-67) steered through the stages 32a-d of the signal path 30 to the transmission

signal destination 12 in order to perform a phase shift delay of the signal. Hong does not teach that this transmission signal is a control signal in a computer system.

III. Delzer discloses a clock signal from a signal source connected to port P1, through delay paths determined by conductors 12 selectively connected by zero ohm connectors 20 in an adjustable delay line phase shifter. A clock signal is an old and well-known control signal, as evidenced by the following definition of a clock provided in the glossary web-site: "Any of several types of timing control devices, or the periodic signals that they generate." [See Google™ Search attachment] and www.tagnet.org/digitalhymnal/en/glossary_a-l.html.

IV. Since Hong and Delzer are both solving the same type of signal propagation problem, wherein a signal needs to be delayed using selected paths determined by zero-ohm connectors or switch contacts, then the use of such an adjustable delay line phase shift circuit for a control signal on a high frequency circuit board, as taught by Delzer, for use in any high frequency application, such as in a computer environment, would have been readily recognized in the pertinent high frequency electronics art of Hong.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the high frequency communication signal in Hong to be a control signal, specifically, the clock signal taught by Delzer, in order to use the various delay paths in Hong for selectively determining the precise phase delay for the control (clock) signal required by the particular electronic application of the delay circuit of Hong, as taught by Delzer.

As to Claim 18, modified Hong further discloses selecting a unique length for each of the first cluster of possible signal paths 34; selecting a unique length for each of the second cluster possible signal paths 58; and selecting said unique lengths for the first and second clusters of possible signal paths such that each combination of the first and second signal paths 34 and 58 have unique lengths (col.4: 58-col.5: 13).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong in view of Delzer and the Google™ Search definition of "clock," as applied to Claim 1, above, and further in view of Osaka et al.

I. Hong, as modified by Delzer, discloses that the control signal source is a clock source and the control signal path is a clock signal path (see rejection of base Claim 1, above). Hong, as modified by Delzer, also teaches a clock signal destination (the output of amplifier 88; see Fig. 7 and co.5: 18-19) but does not identify a specific control signal destination; i.e., does not teach that the control signal destination is, for example, a memory controller wherein the memory controller uses a clock signal propagating on the clock signal path as a read clock for reading data from a memory bus.

II. Osaka et al. discloses a source-clock-synchronized memory system wherein the memory controller uses a clock signal propagating on a clock signal path as a read clock for reading data from a memory bus (col.11: 58-col.12: 6 and col.12: 38-44).

III. Since the delay circuit of Hong, as modified by the clock delay circuit of Delzer, teaches a clock source and a clock signal path with calibrated delay, then the use of such a calibrated source clock signal by a memory controller in a computer system as a read clock for reading data from a memory bus, as taught by Osaka et al.,

would have been readily recognized as an application of the phase shifter that performs a calibrated delay of the clock signal in the pertinent art of modified Hong.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Hong, as modified by Delzer, by directing the selectively delayed control signal of modified Hong to a control destination that is a memory controller, wherein the memory controller uses a clock signal propagating on the clock signal path as a read clock for reading data from a memory bus, thereby using the phase shifted clock signal of Hong, as modified by Delzer, in a memory system of a computer, as taught by Osaka et al.

6. Claims 27, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong in view of Delzer, the above-cited definition of "clock" found on Google™ and LaBerge.

A) As to Claim 27:

I. Hong discloses, in Fig. 3: an adjustable signal delay circuit 30 coupled between a signal source (connected to input line 40; col.4: 3: 65-66) and a signal destination (radiating element) connected to output line 12 (col.4: 54-57), the adjustable signal delay circuit 30 delays a source signal (col.4: 29-57), the adjustable signal delay circuit 30 comprising: a first plurality of signal paths 34a,b,c each having two ends, a source end of a selected (i.e., any one) path of the first plurality of signal paths 34a,b,c, coupled to the signal source (through input line 40; Fig. 3 and col.4: 6-11); a second plurality of signal paths 58a,b,c (the designations a,b,c added by the Examiner and corresponding to each line of stage 32d, as in lines 34a,b,c in stage 32a) each having two ends, a

destination end of a selected (i.e., any one) path of the second plurality of signal paths 58a,b,c, coupled to the signal destination (Fig. 3; col.4: 54-57 and col.5: 1-11); a spanning circuit (stages 32b and 32c) coupling the selected path of the first plurality of signal paths 34a,b,c to the selected path of the second plurality of signal paths 58a,b,c (Fig. 3 and col.4: 44-57); and wherein the length of the signal path through the adjustable signal delay circuit 30 is at least the sum of a length of the selected path of the first plurality of signal paths 34a,b,c and a length of the selected path of the second plurality of signal paths 58a,b,c (Fig. 3).

IIa. Hong teaches a transmission signal from the signal source at input line 40 (col.3: 63-67) steered through the stages 32a-d of adjustable signal delay circuit 30 to the transmission signal destination 12 in order to perform a phase shift delay of the signal. Hong does not teach that this transmission signal is a control signal in a computer system.

IIb. Delzer discloses a clock signal from a signal source connected to port P1, through delay paths determined by conductors 12 selectively connected by zero ohm connectors 20 in an adjustable delay line phase shifter. A clock signal is an old and well-known control signal, as evidenced by the following definition of a clock provided in the glossary web-site: "Any of several types of timing control devices, or the periodic signals that they generate." [See Google™ Search attachment] and www.tagnet.org/digitalhymnal/en/glossary_a-l.html.

IIc. Since Hong and Delzer are both solving the same type of signal propagation problem, wherein a signal needs to be delayed using selected paths determined by

zero-ohm connectors or switch contacts, then the use of such an adjustable delay line phase shift circuit for a control signal on a high frequency circuit board, as taught by Delzer, for use in any high frequency application, such as in a computer environment, would have been readily recognized in the pertinent high frequency electronics art of Hong.

IId. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the high frequency communication signal in Hong to be a control signal, specifically, the clock signal taught by Delzer, in order to use the various delay paths in Hong for selectively determining the precise phase delay for the control (clock) signal required by the particular electronic application of the delay circuit of Hong, as taught by Delzer.

IIIa. Hong and Delzer teach an adjustable signal delay circuit for use in a high frequency signal environment, wherein any type of signal, including a control (clock) signal for use in a computer environment, can be selectively delayed for precise and reliable functional interaction with its destination device. However, neither Hong nor Delzer disclose a particular computer system environment with specific control signal sources and destinations to which the disclosed adjustable signal delay circuit is applied.

IIIb. LaBerge discloses a computer system environment having control signal sources and destinations (Fig. 6), the computer system comprising: a microprocessor 32 coupled to a primary bridge device 34; a main memory array 44 coupled to a memory controller 70 by way of a memory bus 41 (Figs. 6 and 7), the memory controller

70 integral with primary bridge device 34 (Fig. 7 discloses the details of primary bridge device 34); a secondary bridge device 36 coupled to primary bridge device 34 by way of a primary expansion bus 38; an input/output controller 54 coupled to secondary bridge device 36 by way of a secondary expansion bus 40; and a keyboard 58 coupled to input/output controller 54. LaBerge teaches a system for effective performance of memory read operations, the system including the use of various control signal sources (e.g., memory controller 70, bus controller 65, I/O controller 54) and control signal destinations by way of bus lines (col.2: 27-50; Figs. 6 and 7).

IIIc. Since Hong and Delzer teach an adjustable signal delay circuit for selectively delaying a control signal and LaBerge teaches a computer system for enhancing memory read operation, the system including the use of various control signal sources and control signal destinations, then the adjustable signal delay circuit for selectively delaying a control signal from a control source to its destination, as taught by Hong and Delzer, would have been readily recognized in the pertinent computer system art of LaBerge for selectively delaying the control signals for precise arrival to their destinations for ensuring the optimal performance of the computer system functions required to enhance the memory read operations taught in the computer system of LaBerge.

IIId. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the adjustable signal delay circuit of Hong modified by Delzer in the particular computer system environment of LaBerge in order to ensure

the reliable timing and performance of the control signals for enhancing the memory reading operations of the computer system of LaBerge.

B) As to Claim 31, Hong, as modified by Delzer and LaBerge teaches the adjustable signal delay circuit of Hong modified by Delzer which has been established as useful by one of ordinary skill in the art at the time the invention was made in the particular computer system environment of LaBerge in order to ensure the reliable timing and performance of the control (clock) signals for enhancing the memory reading operations of the computer system of LaBerge (see rejection of base Claim 27, above). Specifically, among the control signal source details featured in the particular computer system of LaBerge to which the adjustable signal delay circuit of Hong modified by Delzer is applied, is that the control signal source is a clock source, the control signal destination is the memory controller 70, the control signal path is a clock signal path, wherein the memory controller 70 uses a clock signal propagating on the clock signal path as a read clock for reading data from the memory bus 41 (col.4: 10-17).

C) As to Claim 32:

I. Hong, as modified by Delzer and LaBerge, teaches a control signal source that is phase shifted for outputting a signal with a calibrated delay for an application (see the rejection of base Claim 1, above) but does not establish the use of a phased lock loop (PLL) as claimed in Claim 32.

II. However, Delzer further discloses, in Fig. 7, that the control signal source is a feedback output (at amplifier 88) of a PLL, the control signal destination (at phase detector 74) is a feedback input of the PLL, the control signal path is a feedback path of

the PLL (the PLL path defined by the path that includes phase shifters 10), and the length of the feedback path (defined by the specific path lengths formed on the adjustable phase shifters 84 and 90) controls a phase relationship between an input signal to the PLL and an output signal of the PLL in order to precisely control the delay of the control signal for an application (Fig. 7; col.4: 61-col.5: 40).

III. Since Hong, as modified by Delzer, are both teaching an adjustable delay line phase shifter for propagating a source control signal to a control signal destination for the purpose of precisely controlling the delay of a control signal for an application, then the establishment of a PLL, the output of which is the control signal source and the input of which is the control signal destination, and the feedback path of which is the control signal path, the length of which path being adjustable and controlling the phase relationship of the input signal to and output signal from the PLL for use in an electronic application requiring such a precisely timed signal, as taught by Delzer, would have been readily recognized for use in conjunction with the adjustable delay line phase shifter in the pertinent art of Hong.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the adjustable delay line phase shifter circuitry of Hong with an added PLL, as taught by Delzer, in order to precisely control the phase relationship between an input signal to the PLL and an output signal of the PLL, as taught by Delzer, for the purpose of outputting a precisely timed signal for use in an electronic application of the adjustable delay line phase shifter circuitry of modified Hong, as taught by Delzer.

Allowable Subject Matter

7. Claims 19-25 and 26 would be allowable if rewritten or amended to overcome the objections set forth above in the present Office action.

8. Claims 2-4, 14-17 and 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 2-4 and 28-30, patentability resides, at least in part, in *a first zero ohm resistor connecting a remaining end of the selected path of the first plurality of signal paths to the medial solder pad*, in combination with the other limitations of the broadest claims, Claim 2 and 28, respectively.

As to Claims 14-17, patentability resides, at least in part, in *coupling a source end of the first signal path to the control signal source using a zero ohm resistor*, in combination with the other limitations of the broadest claim, Claim 14.

As to Claims 19-25, patentability resides in **the combination of** *a first spanning circ0uit coupling the selected first path to a selected third path of the third plurality of signal paths* **and** *a second spanning circuit coupling the selected third path to the selected second path*, in further combination with the other limitations of base Claim 19.

As to Claim 26, patentability resides, at least in part, in *a solder pad coupled to the first device and a zero ohm resistor connecting the solder pad to the first signal path*, in combination with the other limitations of the claim.

10. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Yao (US 5,578,976) is incorporated by reference into Hong (US 6,281,838), which has been relied upon for the rejections set forth above, and teaches the very low resistance (approximately zero ohms) MEM switches used in Hong to determine the selected path length for the signal (col.1: 18-21, 35-38 and 45-48; col.2: 16-21; col.6: 31-32).

b) Venaleck et al. (US 4,906,987) discloses describes zero ohm resistors in the form of switches (col.6: 6-10 and 20-23).

c) Gayle (US 5,801,601) discloses an adjustable delay line circuit using zero ohm resistors to select the delay path (Figs. 1-3; col.2: 29-48).

d) Jean-Frederic (US 4,313,095) discloses an adjustable delay line circuit using zero ohm resistors to select the delay path (Abstract; Figs. 2-8).

e) Rueda-Aguilocho et al. (US 6,274,824 B1) discloses multiple signal/destination paths defined by zero ohm resistors selectively connecting contacts (Figs. 7-17; col.6: 53-65).

f) The following references disclose selecting signal paths by means of zero ohm resistors:

Yoon et al. (US 6,233,157 B1): Figs. 4 and 6; col.4: 46-51.

Mitani et al. (US 5,847,985): Fig. 5; col.6: 39-44 and 55-57.

Kurokawa et al. (US 5,542,049): col.5: 37-44.

Ikeda et al. (US 5,987,531): Figs. 4-6; col.6: 50-col.8: 62.

Takaishi et al. (US 5,418,455): Figs. 1a,b; col.3: 56-59; col.4: 7-24.

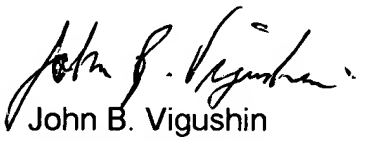
Singer (US 5,805,428): Figs. 4 and 7A,B,C; col.3: 16-30; col.4: 10-17.

Weigler et al. (US 5,224,022): Figs. 4A,B and 5-7; col.5: 32-38.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
March 06, 2005